CLAIMS:

- 1. An apparatus for testing an integrated circuit of a device under test by monitoring an analog signal and a digital signal outputted from the integrated circuit, comprising a comparator, a memory for receiving an output signal from said comparator, a driver for receiving an output signal from said memory, an adder or subtractor which may accept an analog signal outputted from the integrated circuit and a signal outputted from said memory, an integrator which accepts an analog signal outputted from said adder or subtractor, a first switch for selectively transmitting an analog signal outputted from said integrator and a digital signal outputted from said integrated circuit to said comparator, and a second switch for selectively transmitting a signal outputted from said memory and a signal outputted from said comparator to said driver, wherein at least one of said switches is operated depending on whether a signal to be tested is analog or digital.
- 2. An apparatus according to claim 1, further comprising a third switch and a digital filter which are connected between said comparator and said memory, for transmitting the signal outputted from said comparator

selectively via said digital filter to said memory.

- 3. An apparatus according to claim 1, further comprising a delay circuit connected between said comparator and said adder or said subtractor.
- 4. An apparatus for testing an integrated circuit of a device under test by monitoring an analog signal and a digital signal outputted from the integrated circuit, comprising a comparator, a memory for receiving an output signal from said comparator, a driver for receiving an output signal from said memory, an adder or subtractor which may accept an analog signal outputted from the integrated circuit and a signal outputted from said driver, an integrator which accepts an analog signal outputted from said adder or subtractor, a first switch for selectively transmitting an analog signal outputted from said integrator and a digital signal outputted from said integrated circuit to said comparator, and a second switch for selectively transmitting a signal outputted from said memory and a signal outputted from said comparator to said driver, wherein at least one of said switches is operated depending on whether a signal to be tested is analog or digital.
 - 5. An apparatus according to claim 4, further

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comprising a third switch and a digital filter which are connected between said comparator and said memory, for transmitting the signal outputted from said comparator selectively via said digital filter to said memory.

- 6. An apparatus according to claim 4, further comprising a delay circuit connected between said comparator and said adder or said subtractor.
- 7. An apparatus according to claim 4, further comprising a delay circuit connected between said comparator and said second switch.
- 8. An apparatus according to claim 4, wherein said driver is disposed in a feedback loop extending from said comparator to said adder or said subtractor.